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As CMOS semiconductor technology strides towards billions of transistors on a single die new problems arise on the way. They are concerned with the - minishing fabrication process features, which a?ect for example the gate-to-wire delay ratio. They manifest themselves in greater variations of size and operating parameters of devices, which put the overall reliability of systems at risk. And, most of all, they have tremendous impact on design productivity, where the costs of utilizing the growing silicon 'real estate' rocket to billions of dollars that have to be spent on design, veri?cation, and testing. All such problems call for new - sign approaches and models for digital systems. Furthermore, new developments in non-CMOS technologies, such as single-electron transistors, rapid single-?- quantum devices, quantum dot cells, molecular devices, etc. , add extra demand for new research in system design methodologies. What kind of models and design methodologies will be required to build systems in all these new technologies? Answering this question, even for each particular type of new technology generation, is not easy, especially because sometimes it is not even clear what kind of elementary devices are feasible there. This problem is of an interdisciplinary nature. It requires an bridges between di?erent scienti?c communities. The bridges must be built very quickly, and be maximally ?exible to accommodate changes taking place in a logarithmic timescale.

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